AMENDMENTS TO THE CLAIMS

Claim 1 (currently amended): A bipolar junction transistor (BJT) comprising:

a substrate;

a dielectric layer formed on a predetermined region of the substrate;

an oxide layer and a silicon nitride layer stacked on the dielectric layer;

an opening formed in the dielectric layer, the oxide layer, and the silicon nitride layer, ~~and~~ a portion of the substrate being exposed;

a heavily doped polysilicon layer formed on a sidewall of the opening and on the substrate to define a self-aligned base region in the opening;

an intrinsic base doped region formed within the substrate and in a bottom of the opening by implanting through the self-aligned base region;

a spacer formed on the heavily doped polysilicon layer to define a self-aligned emitter region in the opening; and

an emitter conductivity layer being filled ~~with~~ into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the intrinsic base doped region.

Claim 2 (original): The bipolar junction transistor of claim 1 wherein the heavily doped polysilicon layer is doped with a boron dopant with a dosage ranging from 1E19 to 1E21 atoms/cm^3.

Claim 3 (original): The bipolar junction transistor of claim 1 wherein the substrate is a silicon substrate.

Claim 4 (original): The bipolar junction transistor of claim 1 wherein the substrate is a non-selective epitaxial silicon substrate.

Claim 5 (original): The bipolar junction transistor of claim 1 further comprising a self-aligned silicide (salicide) layer formed on the emitter conductivity layer.

Claim 6 (original): The bipolar junction transistor of claim 1 further comprising a selective implant collector (SIC) region formed in the substrate beneath the intrinsic base doped region.

Claim 7 (currently amended): The bipolar junction transistor of claim 1 further comprising an extended conductivity layer formed on the silicon nitride ~~dielectric~~ layer electrically connected to the heavily doped polysilicon layer.

Claim 8 (canceled)

Claim 9 (original): The bipolar junction transistor of claim 7 wherein the extended conductivity layer is composed of in-situ doped polysilicon.

Claim 10 (canceled)

Claim 11 (currently amended): A hetero-junction bipolar

junction transistor (HBT) comprising:

a substrate;

a dielectric layer formed on a predetermined region of the substrate;

an opening formed in the dielectric layer, and a portion of the substrate being exposed;

a SiGe epitaxial layer formed on a sidewall and a bottom of the opening, and extending outside the opening and above the dielectric layer;

a spacer formed on the SiGe epitaxial layer to define a self-aligned emitter region in the opening; and

an emitter conductivity layer being filled ~~with~~ into the self-aligned emitter region, and a PN junction being formed between the emitter conductivity layer and the SiGe epitaxial layer.

Claim 12 (original): The hetero-junction bipolar junction transistor of claim 11 wherein the substrate is a silicon substrate.

Claim 13 (original): The hetero-junction bipolar junction transistor of claim 11 wherein the substrate is a non-selective epitaxial silicon substrate.

Claim 14 (original): The hetero-junction bipolar junction transistor of claim 11 further comprising a self-aligned silicide (salicide) layer formed on the emitter conductivity layer.

Claim 15 (original): The hetero-junction bipolar junction transistor of claim 11 further comprising a

selective implant collector (SIC) region formed in the substrate beneath the SiGe epitaxial layer.

Claim 16 (canceled)

Claim 17 (canceled)